causing current leakage therethrough while maintaining high resistance.

The Patent Office states that in Wang isolators 14 and isolator control $\phi 3$ are the high resistance controllable current leakage imperfect isolating means.

Applicant defines in claim 1 means for applying an enabling voltage for causing effective current to leak through the imperfect isolating means. The Patent Office states that the enabling voltage $\phi 3$ constitutes this element.

However, Wang, in column 2, lines 37-39 defines isolating transistors 14 and isolating signal $\phi 3$ that turns each isolating transistor off.

Wang in column 3, lines 52 and 53 teaches that the isolating signal $\phi 3$ disconnects the half of bit line 10.

Webster's New Collegiate Dictionary, copyright 1977 defines "isolate" as "to separate from another substance so as to obtain pure or in a free state". A synonym is "insulate".

It is submitted that the reference is crystal clear in that transistors 14 are taught to totally insulate one side of the bit line 10 and 12 from the other. There is no imperfect isolating means described for causing current leakage through it while maintaining high resistance, as defined in applicant's claim 1.

There is no means taught in the reference for applying an enabling voltage for causing effective current

to leak through the high resistance imperfect isolating means as defined in applicant's claim 1. Indeed, Wang teaches the opposite: a perfect isolator with no possible current leakage through a high resistance.

There is no means taught in the reference for disabling an imperfect isolating means, thereby removing isolation between sense nodes and the bit line as defined in applicant's claim 1. The only means taught is disabling a perfect isolating (insulating) means.

It is clear from what is stated in Wang that the isolating signal $\phi 3$ disconnects the bit line or allows connection between the halves of the bit line. There is no current leakage through FETs 14, since Wang clearly states that the bit line is disconnected. It is not seen how in any way a disconnection can cause current leakage, as defined by applicant. Disconnection causes cessation of passage of any current.

Clearly in applicant's claim 1 there is defined two states of applicant's isolating means: a state in which there is current that leaks through a high resistance, and a state in which the imperfect isolation is removed (i.e. that there is a low resistance conductive path between the sense nodes and the bit line). Nothing similar is described in Wang. The elements called out by the Patent Office clearly do not comprise the elements defined by applicant, nor do they function in a similar manner.

Applicant incorporates by reference his comments above in respect of the remaining rejected claims.

In the event that the Patent Office again rejects the claims in view of Wang, it is respectfully requested to respond to the specific issues raised above, and to advise the applicant where Wang describes, and how, element 14 and the voltage $\phi 3$ provide both a high resistance leakage path under control of an enabling voltage which causes effective current to leak through the high resistance isolating means, as defined in clause (d) of claim 1, and means for disabling an imperfect isolating means thereby removing isolation between the sense nodes and the bit line as defined in clause (g) of claim 1, particularly in view of the clear direction in column 3, lines 52 and 53 of Wang that the bit line is disconnected by means of the isolating signal $\phi 3$. In the event that the Patent Office construes the word "disconnect" as allowing current leakage through a high resistance under control of an enabling voltage, authority and support for this position is respectfully requested.

Withdrawal of the rejection of all of the claims based on Wang is respectfully requested.

Claims 1-17 were rejected as anticipated by either of the Miyamoto et al references. Applicant respectfully traverses the rejection for the following reasons.

Miyamoto et al '850 states in column 10, lines 33-38 that the divided bit lines are connected to each other through MOSFETs Q14 and Q15, which are turned on by a signal TR. MOSFETs are well known to be isolating when turned off (i.e. as described by Wang), and fully conducting when "turned on". As is clear by a thorough reading of either of the Miyamoto et al patents, the FETs are used as switches. There is not a single suggestion or teaching in the reference that FETs Q14 and Q15 have a high resistance state that includes current leakage and imperfect isolation. The transistors are clearly used alternately as virtually perfect conductors or virtually perfect isolators, as implied in column 10, lines 33-38, wherein it states that the divided bit lines are connected to each other through a MOSFET Q14.

Similar language is used in Miyamoto et al '663, column 2, lines 46-52, wherein it states that divided bit lines are connected to each other through a transfer gate, and that transfer gates are turned on in response to a transfer signal.

There is not a single suggestion or teaching in the reference that the transfer gates have a high resistance state that includes current leakage and imperfect isolators, or that there is any means for applying an enabling voltage for causing effective current to leak through the imperfect isolating means, and means for disabling the imperfect isolating means, thereby removing isolation between the

sense nodes and the bit line, as defined in applicant's claims.

Clearly applicant's invention is not described in either of the Miyamoto et al references. Withdrawal of the rejection of claims 1-17 is therefore respectfully requested.

In the event the Patent Office reapplies the Miyamoto et al references, it is respectfully requested to advise where, exactly and how the references teach the specific elements of applicant's claim 1, clauses (d), (e) and (g).

The comment in Paper No. 17, in paragraph numbered 7, that the newly added means is found in Wang as indicated in paragraph (5) of the office action is not understood. Paragraph (5) references to isolators and isolator control. The isolators in the references are not high resistance controllable current leakage imperfect isolating means, as defined in applicant's claims but are switches, having no current leakage therethrough. As noted above, isolation (not imperfect isolation) is directly contrary to what applicant has claimed. Applicant has claimed a controllable resistance having two states, one which current leaks between the bit line and the sense nodes, and the other in which the imperfect isolation is removed, thereby providing a conductive path, the latter state only being equivalent to the isolators of Wang and Miyamoto et al when they are "turned on".

In essence, in the references, when the isolators are "turned on", they disable the isolation, thereby removing isolation between the parts of the bit line. However when they are turned off, they isolate, i.e. insulate as defined in the dictionary. In contrast, in applicant's invention when they are not "turned on" and when an enabling voltage is applied, there is effective current that leaks through the high resistance imperfect isolating means, which is completely different from that described in the reference. This difference is at the heart of the significant structure, operation and result of applicant's invention, with respect to that of the reference, and is clearly different from and is not taught or implied in the references.

In the event that the Patent Office considers that there is allowable subject matter contained in this application, but that the differences between the Patent Office and the applicant are to the particular language used in the claims to define the high resistance controllable current leakage imperfect isolating means or other elements, the Examiner is invited to telephone the undersigned at (703)312-6600, whereupon a resolution satisfactory to both the Patent Office and to the applicant may be resolved.

It is believed that this application is in form for allowance. Notice of allowance is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (628.30050CX1) and please credit any excess fees to such deposit account.

Respectfully submitted,

Donald R. Antonelli
Registration No. 20,296
ANTONELLI, TERRY, STOUT & KRAUS

DRA/cec
(703) 312-6600